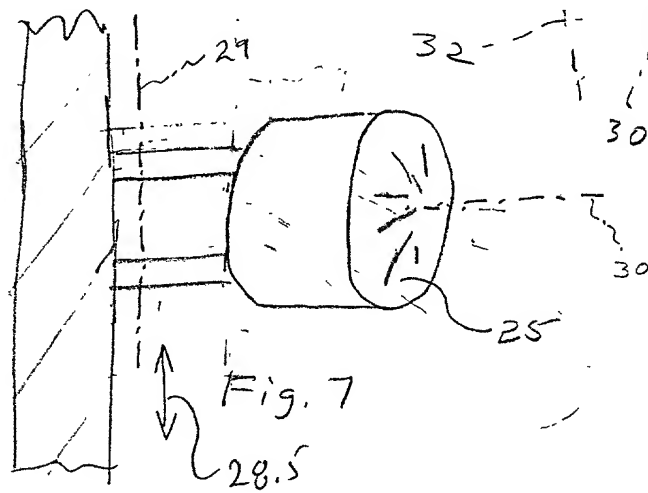
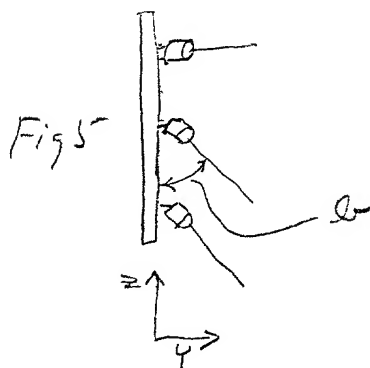
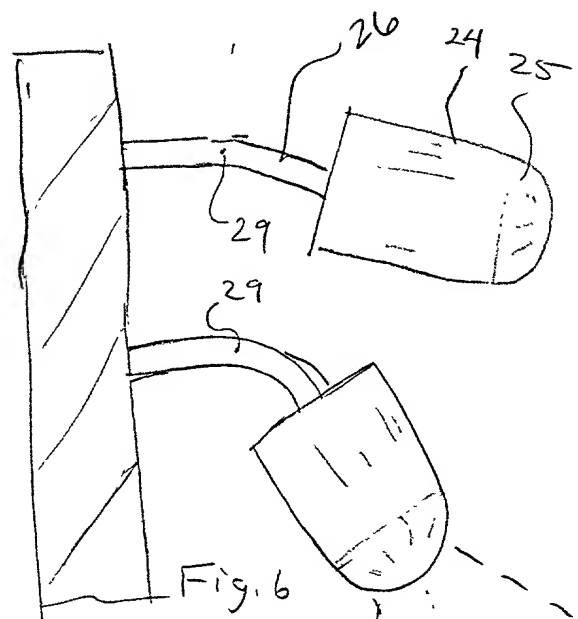
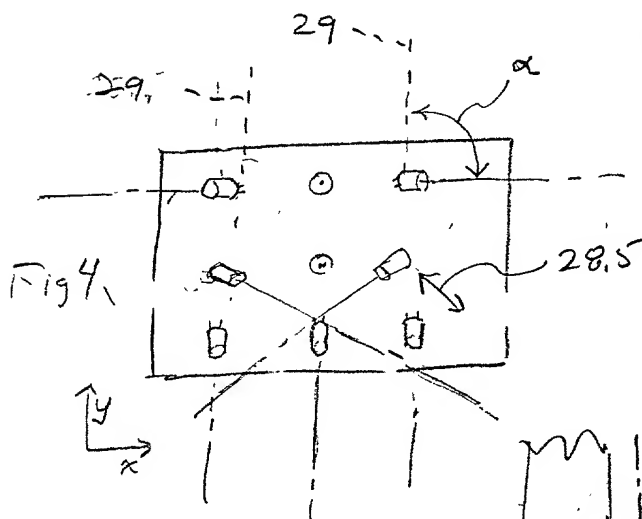
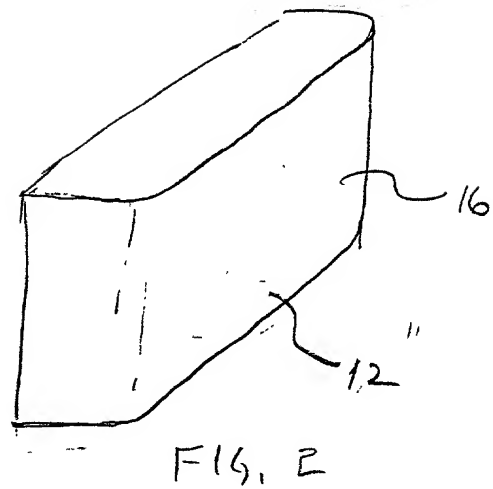
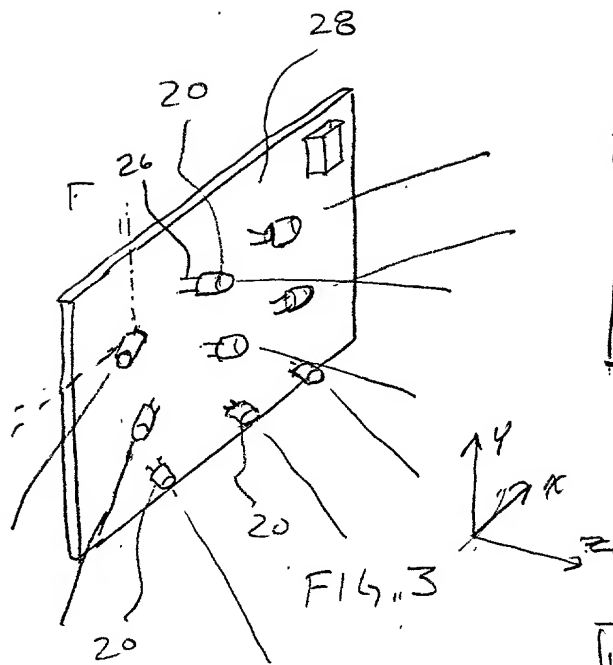
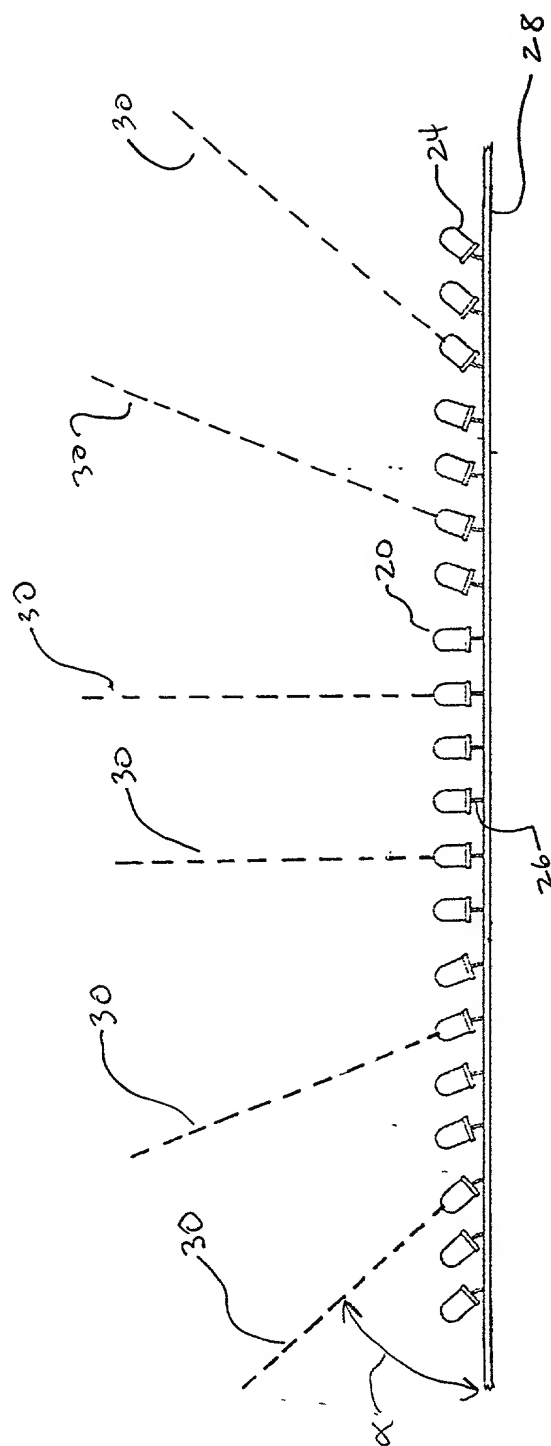


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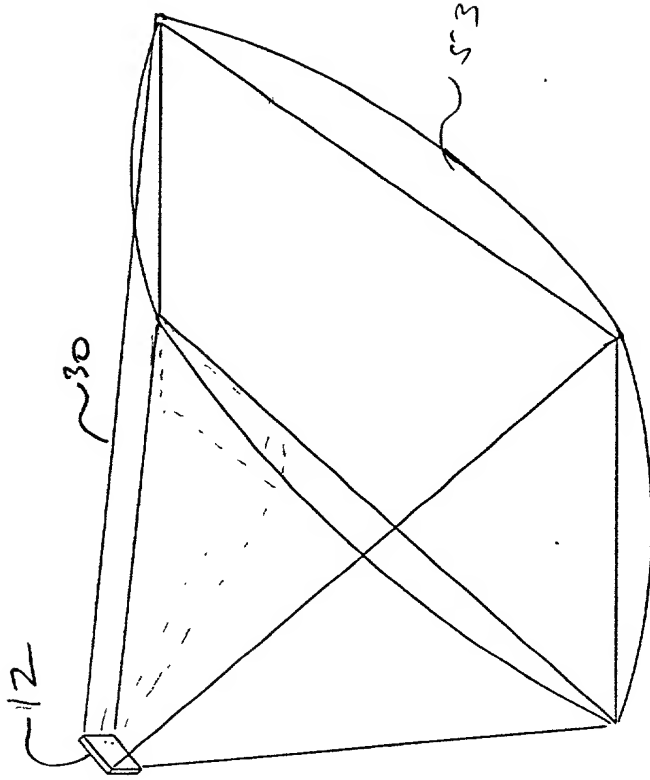
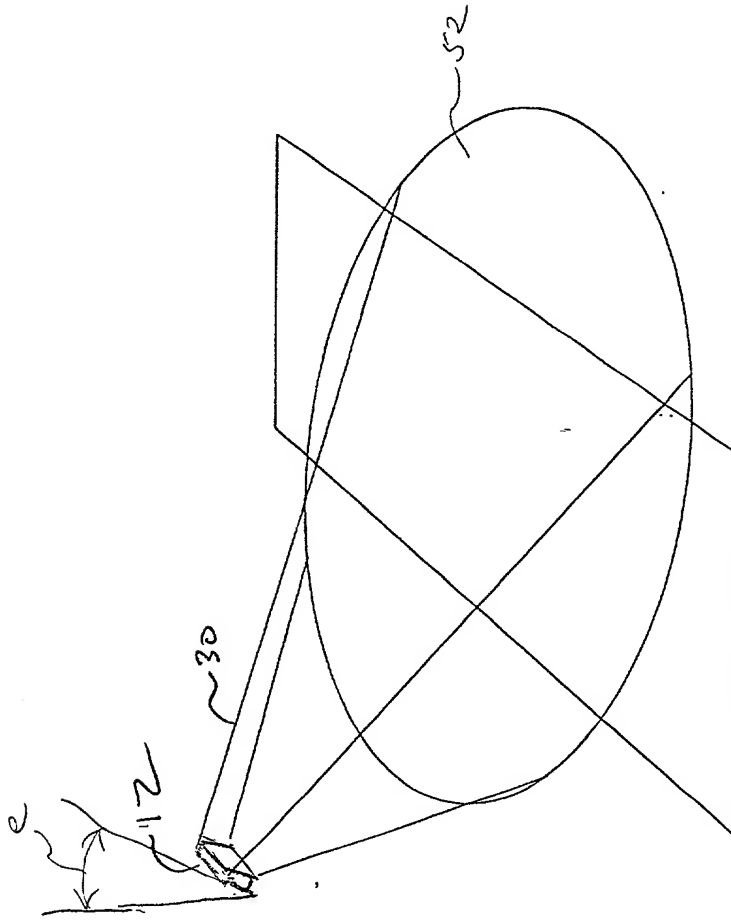


Fig. 9
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Fig. 10

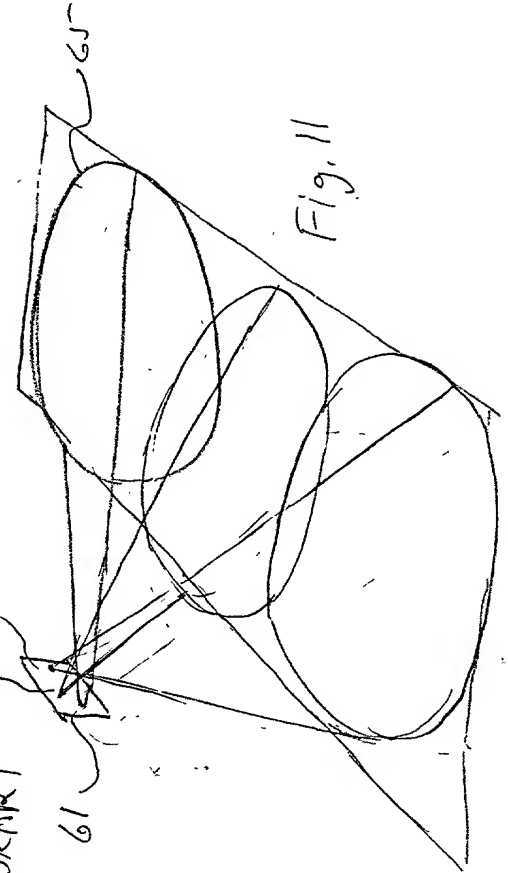


Fig. 11

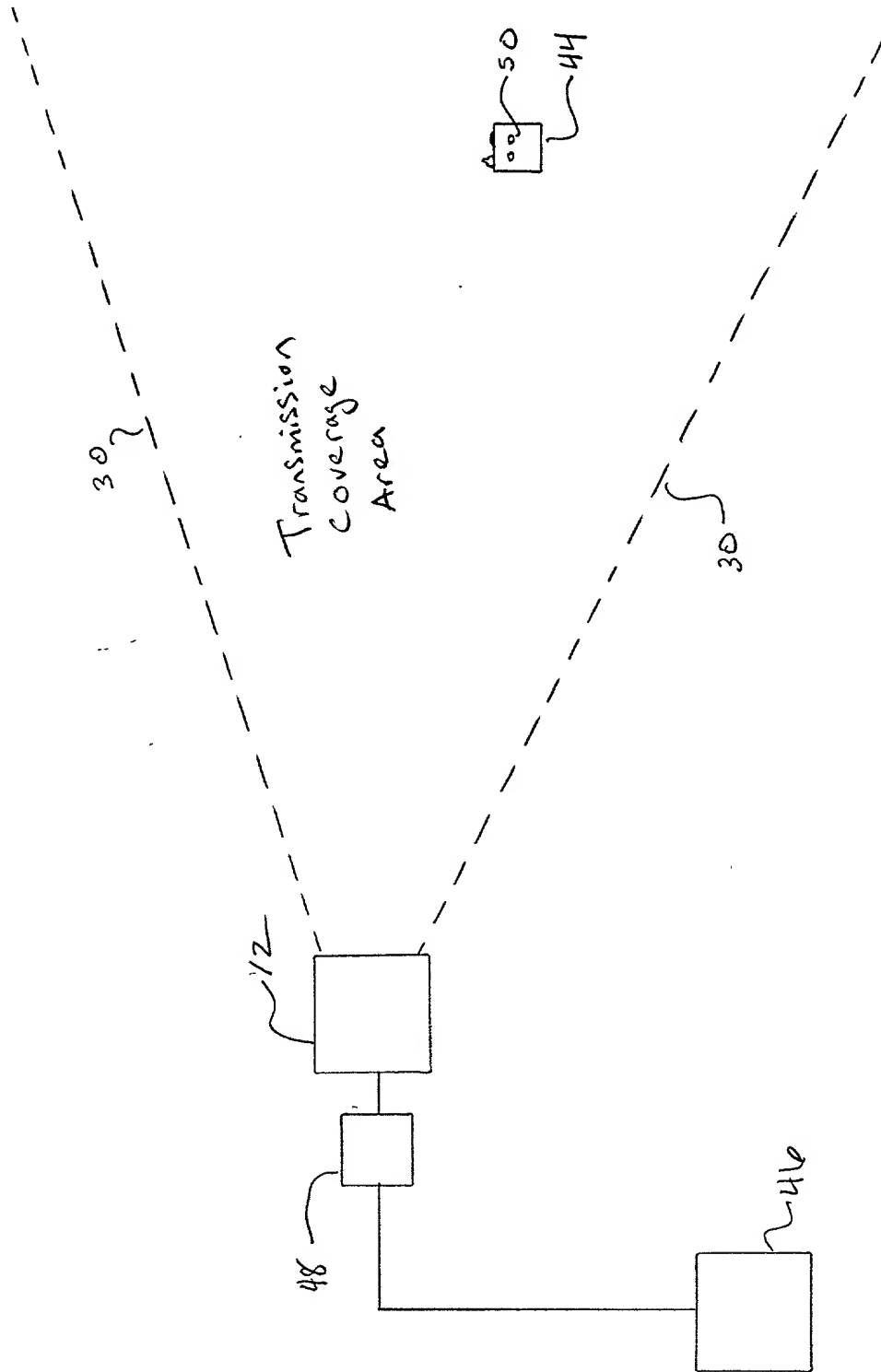


Fig 12

FIG. 13 is a block diagram of a system 100 for providing a visual indication of a status of a system. The system 100 includes a processor 102, a memory 104, a display 106, and a user interface 108. The processor 102 is configured to receive input from the user interface 108 and to control the display 106 to display a visual indication of the status of the system. The memory 104 is configured to store data and instructions for the processor 102. The display 106 is configured to display the visual indication of the status of the system. The user interface 108 is configured to receive input from a user and to provide output to the user.

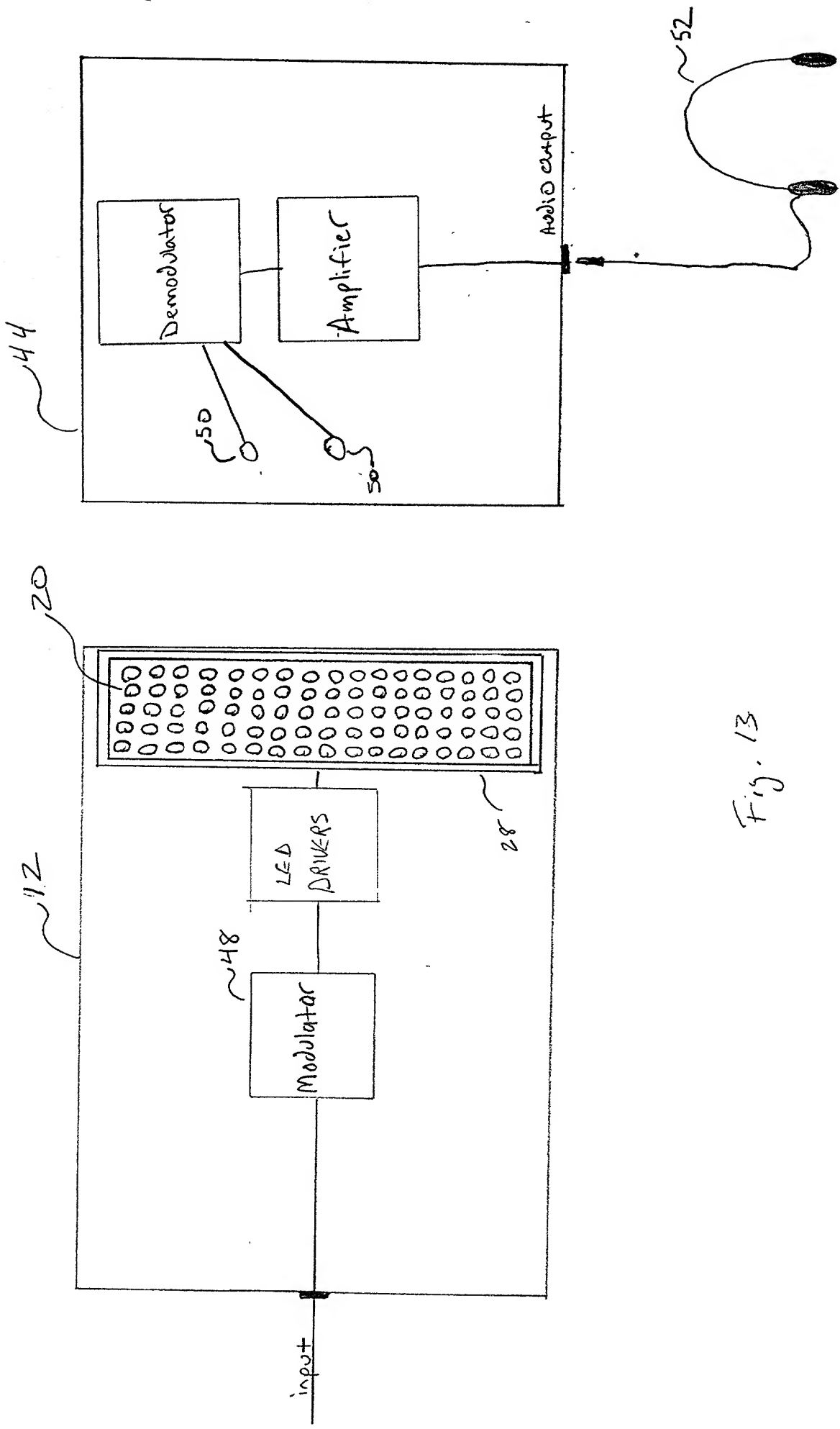


Fig. 13

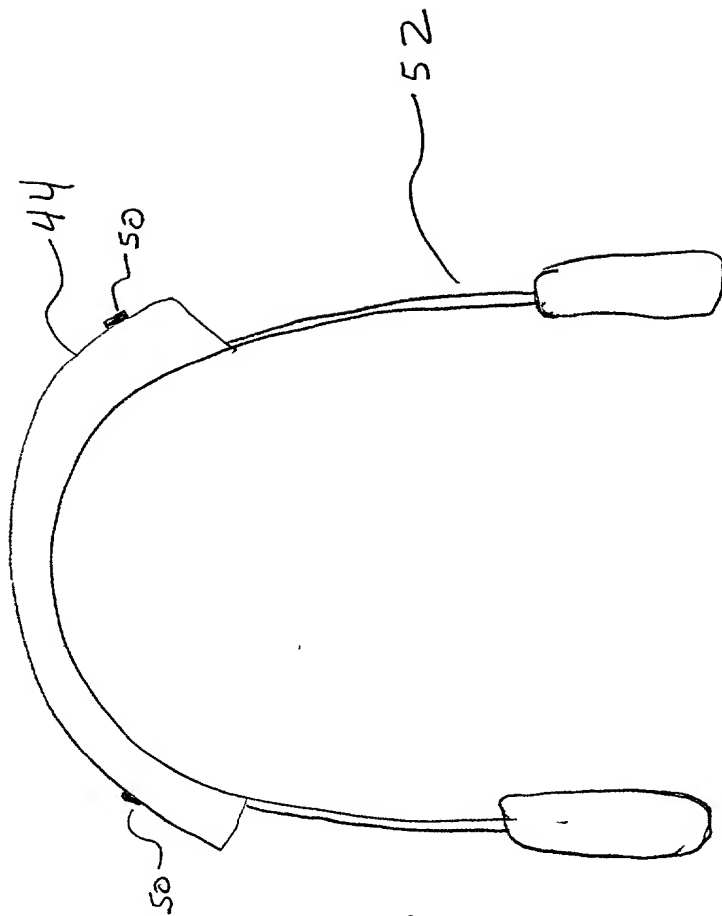


Fig. 14